What is claimed is:

1. A semiconductor memory device comprising: a plurality of RAMs of differing memory space sizes on the same substrate; and means for setting the number of address signals in each of said plurality of RAMs equal to the number of address signals in the largest address space.

2. A semiconductor memory device comprising: a plurality of RAMs of differing memory space sizes on the same substrate; and means for setting the number of address signals in each of said plurality of RAMs equal to the number of address signals in the largest address space when mapping the address space for test purposes.

3. A semiconductor memory device comprising: a plurality of RAMs of differing memory space sizes provided on the same substrate; and means capable of changing an address connection between an external input address and a chip internal input address according to said differing memory spaces, wherein said means enables the number of address signals in each of said plurality of RAMs to be set equal to the number of address signals in the largest address space.

4. A semiconductor memory device as set forth in claim 3, wherein said means capable of changing an address connection between an external input address and a chip internal input address is placed before a position at which

an external input address signal is converted to an internal address signal.

5. A semiconductor memory device as set forth in claim 3, wherein said means capable of changing an address connection between an external input address and a chip internal input address is placed after a position at which an external input address signal is converted to an internal address signal.

6. A semiconductor memory device as set forth in claim 3, wherein said means capable of changing an address connection between an external input address and a chip internal input address is a physical or electrical means.

7. A semiconductor memory device as set forth in claim 6, wherein said means capable of changing an address connection between an external input address and a chip internal input address is an electrical means, and includes an address shift means for shifting, in response to a connection change made for a designated address, all addresses higher or lower than said designated address.

8. A semiconductor memory device as set forth in claim 6, wherein said means capable of changing an address connection between an external input address and a chip internal input address is an electrical means, and includes an address shift means for shifting said address connection to a higher order position or a lower order position until

a desired connection is established between said external input address and said chip internal input address.

9. A semiconductor memory device as set forth in claim 6, wherein said means capable of changing an address connection between an external input address and a chip internal input address is an electrical means, and is constructed from a switch that is controlled by a signal.

10. A semiconductor memory device as set forth in claim 9, wherein an external or internal signal capable of recognizing a difference in memory space is used to control said signal for controlling said switch.

11. A semiconductor memory device as set forth in claim 7 or 8, wherein said address shift means includes means for fixing said chip internal input address to a high or a low level when said chip internal input address is disconnected from said external input address.

12. A semiconductor memory device comprising: a plurality of RAMs of differing memory space sizes provided on the same substrate; means for applying the same mapping to said differing memory spaces when simultaneously testing said plurality of RAMs; and means for inhibiting access to each individual RAM according to said differing memory spaces.

13. A method for testing a semiconductor memory device having a plurality of RAMs of differing memory space

sizes on the same substrate, wherein all of said RAMs are tested simultaneously by setting the number of address signals in each of said plurality of RAMs equal to the number of address signals in the largest address space.